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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARRELL, ROBERT B	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,706	SCHINAZI, STEPHANE	
	Examiner	Art Unit	
	Robert B. Harrell	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-21 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-21 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *see attached Office Action*.

1. Claims 15-21 and 23-28 remain presented for examination.

2. The Foreign Priority Documents have not been filed and the Japanese copies are in error as they belong to another application.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The applicant should always use this period for response to thoroughly and very closely proof read and review the whole of the application for correct correlation between reference numerals in the textual portion of the Specification and Drawings along with any minor spelling errors, general typographical errors, accuracy, assurance of proper use for Trademarks ™, and other legal symbols ®, where required, and clarity of meaning in the Specification, Drawings, and specifically the claims (i.e., provide proper antecedent basis for "the" and "said" within each claim). Minor typographical errors could render a Patent unenforceable and so the applicant is strongly encouraged to aid in this endeavor.

5. Each claimed feature must be shown in the figures or the features must be cancelled.

6. The following is a quotation of the second paragraph of 35 U.S.C 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. ***Claims 15-21 and 23-28 are rejected under 35 U.S.C 112, second paragraph***, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The scope of meaning of the following claim language is not clear:

a) "the internal network equipment"--claim 25 (line 4);
b) "the gateway function"—claim 25 (last line).

8. As to 7 (a and b) above, these are but a few examples of numerous cases where clear antecedent basis are lacking and not an exhausting recital. Any other term(s) or phrase(s) over looked by examiner and not listed above which start with either "the" or "said" and do not have a single proper antecedent basis also is indefinite for the reasons outlined in this paragraph. Also, these are but a few examples where term(s) or phrase(s) are introduced more than once without adequate use of either "the" or "said" for the subsequent use of the term(s) or phrase(s). Moreover, multiple introduction of a term, or changes in tense, results in a lack of clear antecedent basis for term(s) or phrase(s) which relied upon the introduced term. Failure to correct all existing cases where clear antecedent basis are lacking can be viewed as non-responsive. Nonetheless, should a response yield all claims allowable short ***a few*** cases where clear antecedent basis are lacking within the claims, a preemptive authorization to enter an examiner's amendment

to the record to correct such would accelerate a notice of allowance over a final rejection. Such could be added at the end of an applicant's response with the following statement: "Examiner is hereby authorized, without the need of further contact by examiner, to enter an Examiner's Amendment to correct any cases where antecedent basis are lacking." if the applicant so elects. This does not diminish the applicant's requirement to correct all such cases not so listed in the example few given above nor prohibit any amendments after a notice of allowance by the applicant.

9. Per claims 17, 18, 19, and 27, and any other claims over looked using the same, "adapted for" and "adapting" language suggests or makes optional but does not require steps to be performed nor limit a claim to a particular structure and thus does not limit the scope of a claim or claim limitation (see MPEP 2106 (II(C))). Therefore, the claim scope is open ended without meets and bounds and thus indefinite.

10. The use of "and/or" fails to establish the meets and bounds of the defined invention because of the variable and dynamic nature of the Boolean operation "and" plus "or". Either the claim contains both or contains only one; and which one is not clearly defined within the claimed invention.

11. The of "(" and ")" leads to confusion with respect to the claims as amended and is not clearly ascertained if "[" and "]" were to be used in place of those so indicated herein.

12. The claims of this application recite, for example in claim 15 (line 4), "including". However, in absence of commas "," it is not clearly ascertained who or what includes the memory and Internet protocols as the claims being with an electronic component comprising a DSP. Thus, giving the claims their broadest reasonable interpretation, the claims recite an electronic component that comprises a DSP and at least one memory and the Internet protocols. The claims do not recite an electronic component comprising a DSP which DSP further comprises at least one memory.

13. Prior to addressing the grounds of the rejections below, should this application ever be the subject of public review by third parties not so versed with the technology (i.e., access to IFW through Public PAIR (as found on **http://portal.uspto.gov/external/portal/pair**)), this Office action will usually refer an applicant's attention to relevant and helpful elements, figures, and/or text upon which the Office action relies to support the position taken. Thus, the following citations are neither all-inclusive nor all-exclusive in nature *as the whole of the reference is cited* and relied upon in this action as part of the substantial evidence of record. Also, no temporal order was claimed for the acts and/or functions.

14. ***Claims 15-21 and 23-28 are rejected under 35 U.S.C. 102 (e)*** as being anticipated by Narasimhan et al. (United States Patent Number: US 6,446,192 B1).

15. The rejection, and grounds for rejection, under 35 U.S.C. 102(e) as presented in examiner's prior Office Action, including citation therein to Narasimhan's figures and

text, are hereby maintained and incorporated in this Office Action by reference herein as given below.

16. Per claim 15 and claim 26, Narasimhan taught an electronic component (e.g., see figure 2) for connection to a telecommunications network (e.g., see col. 5 (line 63-et seq. "Internet" and/or "modem" anticipated "telephones" as covered in col. 6 (line 12 "phone lines")) and data exchange in accordance with at least a part of Internet protocols (e.g., see figure 2 "TCP" and/or "IP" and/or FTP and/or HTTP and/or SMTP exc...), comprising a DSP (Digital Signal processor) (e.g., see col. 6 (line 21 and line 30)) including at least one memory (e.g., see Abstract, figure 2, and figure 12) in which is loaded a program implementing the Internet protocols including routines for message handling (e.g., see figure 2 (SMTP), FTP download (e.g., see figure 2 "FTP")), and/or Web server functionalities (e.g., see figure 2 ("HTTP")), the DSP further comprising a signal processing program for exchange of data on the network (e.g., see figure 12 and col. 6 (lines 47-59). In short, Narasimhan placed Internet functionality onto a single integrated monolithic processor based modem chip. Web pages contain digital signals (music, voice, movies), thus accessing such pages and processing them was also digital signal processing (DSP) per col. 6 (line 21).)). Also, figure 2 recited more Internet protocols such as IP and TCP per col. 6 (lines 47-59) for PPP and figure 12's buffers (70) for intermediate calculations.

17. Per claim 16, claim 17, claim 18, claim 19, and claim 20 see col. 6 (lines 9 ("modem" required A/D (analog to digital converters and modems had DSPs in col. 6 (line 21)), col. 6 in line 12 "phone line" anticipated and/or encompasses POT / switched telephone network or cell phones that had DSP, col. 6 in line 13 "radio", such as walky-talkies that had DSPs, all of which where electric networks as was Ethernet of col. 6 (line 47)).

18. Per claim 21, size is a design choice anticipated in col. 6 (lines 14-29).

19. Per claim 23, claim 24 and claim 25, Internet had Internet providers and the single integrated monolithic processor based Internet modem chip, covered herein, per col. 3 (line 9-et seq.) and col. 5 (line 46-et seq.) with respect to the several Operating System types as supervisory layers for controlling the recited functions and possible receipt of an electronic message ("e-mail" covered in col. 6 (line 52)) with call back login functions using anticipated Internet NAT functions and DHCP per figure 2 (center left) on a computer (by definition a computer was a calculator) encompassed and anticipated by col. 6 (lines 14-29 (i.e., a TI calculator with USB connection)). Internet protocols included within the set Void which required DSP and other voice based protocols that required DSPs and thus built into the chip to cover that Internet protocol as expected by Narasimhan who covered all Internet protocols even if only some were specifically mentioned; and, within the set of all Internet protocols were voice based and thus more unique DSP inherently required.

20. Claim 27 and claim 28, these claims do not teach or defined above the correspondingly rejected claims given above, and are thus rejected for the same reasons given above. That is, Narasimhan taught a single integrated monolithic computer processor based modem chip that performed all known Internet function with known Internet protocols for telecommunication equipment such as voice and thus DSP was inherently required or argued present as the chip performed digital signal processing itself.

21. The applicant respectfully submitted, in his 27 December 2005 response, that US '192 fails to disclose, either explicitly or implicitly, that the program implementing the Internet protocols is loaded in the memory of a DSP. In particular, the SMTP, FTP and HTTP routines of Fig. 2 of US '192 are stored in the Network interface chip 36. This is not a DSP as specifically recited in claim 15. As noted in US ' 192 at column 6, lines 14-21, the device control circuitry 38, which may include a DSP according to line 21, has little or no networking capability. Also, in Fig. 12 of US '192, a UART (Universal Asynchronous Receiver/Transmitter) is used to connect chip 36 to a modem. Thus, chip 36 cannot be considered to be a modem chip inasmuch as it does not comprise modem functionalities. US '192 teaches that the chip cannot be considered as a DSP in which is loaded a program for exchange of data on the network since it is clearly not a DSP and it does not comprise a program for exchange of data on a network. The DSP as recited in Claim 15 is sharply contrasted to US '192 since it comprises a memory in which is loaded Internet protocols and a signal processing program for exchange of data on a network. US '192 does not explicitly or implicitly disclose a DSP comprising such programs. The DSP of US '192 disclosed in column 6, line 21 is in the device control circuitry 38 and does not comprise a memory in which is loaded Internet protocols. The Applicant therefore respectfully submits that US '192 is inapplicable to Claims 15-21 and 23-28 under 35 U.S.C. 102. Withdrawal of the rejection is respectfully requested. ***However***, as indicated above, the amended claims indefinably define if the memory is within the DSP or the electronic device that also contains the DSP as the word "including" could refer to either the DSP or the claimed electronic component.

22. **The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this office action:**

a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. ***Claims 15-21 and 23-28 are rejected under 35 U.S.C. 103(a)*** as being unpatentable over Narasimhan et al. (United States Patent Number: US 6,446,192 B1).

24. The above mapping/citations for rejecting the claims under 35 U.S.C. 102(e) continue and are hereby incorporated into this rejection, under 35 U.S.C. 103(a), by reference. However, it would have been obvious to those skilled in the data processing art to integrate the whole of the circuitries of figure 1B into a single integrated monolithic chip because such was reduce chip count, pin I/O, and size for the same reasons Personal Computers do not take up the area of a 10 story buildings or several city blocks. Furthermore, it would have been obvious to incorporate the network interface chip into such devices as a radio based cell phone per in col. 6 (line 1-et seq.) and thus clearly obvious to integrate the whole of all circuitry onto on a single chip for a single board within the cell phone. That is, per figure 1B, the device 34 being a cell phone could have all of its circuitry 38 and/plus network interface 36 placed/built onto one single monolithic integrated circuit chip because such would reduce chip count, pin I/O, and overall size. Integrating known circuitries is not novel and does not comprise a step towards an invention.

25. The Applicant acknowledges, in his 27 December 2005 response, the rejection of Claims 15-28 under 35 U.S.C. 103 over US '192 by arguing that the applicant's claim 15 recites, among other things, that the memory in which is loaded a program implementing Internet protocols is the memory of a DSP. The Applicant respectfully submits that there is utterly no teaching or suggestion for one skilled in the art to modify US '192 and integrate the whole of the circuitry of Fig. 1b and the network interface functionalities into the memory of a DSP as recited in Claim 15. This is evidenced by the fact, as noted by the Applicant in the Applicant's Specification, that in paragraph [0041], those skilled in the art knew at the time of the invention that the memory of a DSP was not sufficient to load Internet functionalities. Thus, with those teachings known in the art as background, there is no suggestion to modify the US '192 structure and incorporate the programs of two separate components into a single DSP. Also, this would have led one of ordinary skill in the art away from such an incorporation because of memory size problems. The rejection relies on the notion that the integration of the circuitries of Fig. lb of US '192 into a single monolithic chip was to reduce chip count, pin 1/0 and size. However, the Applicant notes that in view of US '192 there is no teaching or suggestion to reduce chip count, pin 1/0 and/or size. IN fact, US '192 teaches a single web interfacing chip and, accordingly, nothing in US '192 teaches or suggests that the data processing functionalities can be integrated into such a chip. Instead, US '192 only teaches a first chip comprising the Internet functionalities and a second chip which can comprise a DSP. In column 6 at lines 14 and 15, US '192 teaches that the device control circuitry 38 implements the main functionality of the device 34, that typically has little or no network capability.' Thus, this teaching is the opposite of the subject matter recited in Claims 15-21 and 23-28 which recites the incorporation of Internet functionalities into a DSP. The Applicant notes that there is no greater evidence of non-obviousness than when the prior art teaches away' from the claimed subject matter. That is exactly the case here wherein US '192 at column 6, lines 14 and 15 teaches away from the subject matter of the solicited claims. As a consequence, the Applicant respectfully submits that all of the claims are non-obvious over US '192. Withdrawal of the 103 rejection is respectfully requested. In light of the foregoing, the Applicant respectfully submits that the entire

application is now in condition for allowance, which is respectfully requested. ***However***, as indicated in col. 3 (line 31-52), in part, the network interface chip is a ***generic*** and versatile chip that is able to connect to any device using serial, parallel, or customized I/O. Although the chip is generic, it can easily be customized for a particular device by storing programs and/or configuration codes in a portion of its on-chip memory. Alternatively, or in addition, additional customized programs and/or configuration codes may be stored in a second chip (i.e., via DSP in element 38 of figure 1b). Thus, since the network interface chip could perform modem functions (as indicated herein above and in the applied reference), then integration of element 34 onto one single monolithic integrated circuit chip would have been obvious to those skilled in the art for the reasons set forth herein above.

26. ***A shortened statutory period for response to this action is set to expire 3 (three) m1onths and 0 (zero) days from the data of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02, 710.02(b)).***

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert B. Harrell whose telephone number is (571) 272-3895. The examiner can normally be reached Monday thru Friday from 5:30 am to 2:00 pm and on weekends from 6:00 am to 12 noon Eastern Standard Time.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew T. Caldwell, can be reached on (571) 272-3868. The fax phone number for all papers is (703) 872-9306.

29. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

ROBERT B. HARRELL
PRIMARY EXAMINER
GROUP 2142